IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	10/805,755	Confirmation No. 1246
Applicant	:	Shinji Kuno	
Filed	:	03/22/2004	
TC/A.U.	:	2181	
Examiner	:	Ernest Unelus	
Docket No.	:	6639P011	
Customer No.	:	8791	

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Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

In response to the Advisory Action mailed April 11, 2008, Applicant would like to request a pre-appeal panel review of the application.

Remarks/Arguments begin on page 2 of this paper.

REMARKS/ARGUMENTS

Claims 1-3, 18-20 and 22-35 are pending in the present application.

This request is in response to the Advisory Action mailed April 11, 2008 and a Final Office Action mailed December 11, 2007. In the Final Office Action, the Examiner rejected claims 1-3, 18-19, 23-25 and 28-33 under 35 U.S.C. §102(e) as being anticipated by Shimizu (U.S. Patent No. 6,609,977). The Examiner further rejected claims 20, 22, 34 and 35 under 35 U.S.C. §103(a) as being unpatentable over Shimizu in view of Witt (U.S. Patent Publication No. 2004/0109005). Applicants respectfully traverse the rejections and contend that the Examiner has not established a *prima facie* case of anticipation and/or obviousness as evident by omissions of one or more essential elements needed for a *prima facie* rejection..

Pre-appeal panel review of the application in light of the remarks/arguments made herein is respectfully requested.

There are several clear errors/omissions in the Examiner's rejections and arguments. The reference number pertains to reference numerals set forth in the cited references in order for the panel to better understand the grounds for rejection.

I. Rejection Under 35 U.S.C. 102(e) – Applicant presents arguments illustrative that the grounds for rejection do not satisfy statutory requirements under 35 U.S.C. §102. Applicant reserves the right to present additional arguments if a formal Appeal is warranted.

A. Independent claim 1

1) Shimizu does not describe the limitation of the "first processor to decode a first stream data including video data and audio data routed over the communication bus." Applicant refers to the Amendments filed March 4, 2008 and October 9, 2007.

Applicant denotes that, as set forth in the Office Action dated July 25, 2007, the first stream data was interpreted by the Examiner as one or more commands responsive to signaling from hand controller (52) of Shimizu. *See page 4 of the Office Action dated July 25, 2007.* Later, in the Final Office Action dated December 11, 2007, the Examiner interpreted the first stream data as the 3D graphics and audio output transmitted from a main processor (110) to a graphics and audio processor (114) of Shimizu. *See page 3 of the Final Office Action.* Both interpretations are incorrect.

Applicant contends that the 3D graphics and audio output transmitted from the main processor (110) cannot constitute the first stream data as claimed. The main processor (110) does not decode the first stream data (3D graphics and audio output) routed over the communication bus. The "communication bus" is interpreted by the Examiner as the bus between the main processor (110) and the graphics and audio processor (114) of Shimizu. *See Figure 2 of Shimizu.* Even if broadly interpreted, this limitation requires the processor to perform a "decode" operation on the 3D graphics and audio output, namely a translation on this data to produce data of a different format. Shimizu fails to teach such an operation. Rather, Shimizu merely discloses the outputting of 3D graphics and audio output by the main processor (110), where any interpretation of

the outputting of data as a decode operation clearly signals the application of impermissible hindsight reconstruction being applied by the Examiner.

Accordingly, Applicant respectfully requests the Review Panel to render a decision allowing the application.

2) Shimizu does not describe the limitation of the "second processor [being] provided with a second stream data including video data and audio data that is received from the drive device without being routed over the communication bus." Applicant refers to the Amendments filed March 4, 2008 and October 9, 2007.

As claimed, the first processor (CPU) is adapted to decode the first stream data (video data and audio data) sent over the communication bus while the second processor is adapted to decode the second stream data (video data and audio data) that is sent from the drive device *without being routed over the communication bus. Emphasis added.* Both the first and second stream data include video data and audio data. With regard to video data and audio data, efficiency of data compression is being improved higher and higher. The more data is compressed, the more a processor takes time to decode the data. Therefore, the first and second processors share the burdensome processes of decoding video data and audio data from completely different data paths. This may also result in reducing the amount of decoded video and audio data flowing through the communication bus, thereby keeping the data traffic in the communication bus relatively small.

Shimizu, however, teaches the use of a single processor (graphics and audio processor 114) that is controlled by main processor (110) to decode images and audio. *See col., 6, line 53 – col. 7, line 3 of Shimizu.* There is no teaching or suggestion of dedicated decode operations for one type of data stream routed over the communication bus and another type of data streams routed without use of (or being routed over) the communication bus.

More specifically, the Examiner explains how audio data for the second stream data is receives from a mass storage access device (106) without being routed over the communication bus (bus between CPU (110) and Graphics and Audio Processor (114). But, the Examiner clearly fails to take into account that the second processor (Graphics and Audio Processor) is to decode the second stream data (both video and audio) that is not routed over the communication bus. While the Examiner makes a convoluted argument of the routing of the second stream of data (audio and video from mass storage access device (106) without the use of the communication bus, Shimizu clearly states, and quoted by the Examiner, that such information must be routed to the CPU (110), and thus, the communication bus must be used..

> ..."Main processor 110 interactively responses to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"[sic]; in other words, the mass storage device 106 is also there to receive video data)".

Accordingly, Applicant respectfully requests the Review Panel to render a decision allowing the application.

B. Independent claim 28

Applicant incorporates the arguments set forth above in traversing the rejection of claim 1. Hence, Applicant respectfully requests the Review Panel to render a decision allowing the application.

C. Dependent claim 23

Shimizu does not describe the limitation of the "graphic controller to convert the decoded first stream data into display video signals and to transmit the display video signals to the second processor over the video bus." Applicant refers to the Amendments filed March 4, 2008 and October 9, 2007.

Upon review, Applicant respectfully submits that Shimizu does not describe a graphic controller, which is interpreted by the Examiner as the graphics and audio (GA) processor 114. The GA processor 114 is claimed to be in communication with the first processor (main processor 110) and the second processor (the GA processor 114 itself). Herein, the graphic controller (GA processor (114)) is claimed to convert the decoded first stream data (3D graphics and audio commands) into display video signals and to transmit the display video signals to the second processor (itself) over the video bus (communication bus between main processor/video encoder 120 and GA processor 114). *See Page 6 of the Office Action.* If such interpretation is followed, the GA processor (114) would be required decode the 3D graphics and audio command and transfer of display video signals back to itself over the video bus, which is clearly not the data path followed by the GA processor (114).

To better understand the inconsistency of this ground for rejection, the components of claim 23 as interpreted by the Examiner are substituted for the claimed elements:

...a graphics and audio processor (graphic controller) in communication with the main processor (first processor) and the graphics and audio processor (second processor), the graphics and audio processor (graphic controller) to convert the decoded 3D graphics and audio commands (first stream data) into display video signals and [the graphics and audio processor (graphic controller)] to transmit the display video signals to the graphics and audio processor (second processor) over the communication bus between main processor/ video encoder and the graphics and audio processor (video bus).

Accordingly, Applicant respectfully requests the Review Panel render a decision allowing the application.

II. Rejection Under 35 U.S.C. §103(a) – Applicant further believes that a *prima facie* case of obviousness has not been established. Applicant reserves the right to present such arguments if a formal Appeal is warranted.

Conclusion

Applicant respectfully requests the Review Panel render a decision allowing the application.

Respectfully submitted,

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Dated: May 12, 2008 By _____

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